# Spin on dopants for high-performance single-crystal silicon transistors on flexible plastic substrates

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Free-standing micro/nanoelements of single-crystal silicon with integrated doped regions for contacts provide a type of material that can be printed onto low-temperature device substrates, such as plastic, for high-performance mechanically flexible thin-film transistors (TFTs). We present simple approaches for fabricating collections of these elements, which we refer to as microstructured silicon ($\mu$s-Si), and for using spin-on dopants to introduce doped regions in them. Electrical and mechanical measurements of TFTs formed on plastic substrates with this doped $\mu$s-Si indicate excellent performance. These and other characteristics make the material potentially useful for emerging large area, flexible 'macroelectronic' devices. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1894611]

Large area, mechanically flexible electronic systems, known as macroelectronics, are attractive for a range of applications in consumer electronics, sensors, medical devices, and other areas.[1–3] A variety of organic, inorganic, and organic/inorganic hybrid materials have been explored as semiconductors for these systems.[4] We recently demonstrated a "top-down" technology for generating single crystal silicon micro/nanoelements (wires, ribbons, platelets, etc., which we refer to collectively as microstructured silicon, $\mu$s-Si) that can be printed onto plastic substrates for high performance thin film transitors.[5] The same strategy can be used with other important semiconductors, such as GaAs, InP, GaN, etc.[6] One of the key characteristics of this approach is its use of high quality, wafer-based sources of the semiconductor, which are grown and processed separately from the plastic device substrate. Here we show that it is possible not only to grow but also to selectively contact dope the semiconductor in steps that are performed independently from the low temperature substrates. We demonstrate, in particular, that spin on doping procedures performed at the wafer level can yield $\mu$s-Si with integrated doped regions. Electrical and mechanical characterization of transistors formed on plastic substrates with these materials illustrates the good performance and excellent bendability that can be achieved.

Figure 1(a) presents schematically the fabrication process for $\mu$s-Si transistors with doped source (S) and drain (D) contacts on PET substrates. The approach uses a solution processable spin-on dopant (SOD) to dope selected regions of the top silicon layer of a silicon-on-insulator wafer (SOI; Soitec unibond with a 100 nm top Si layer and 200 nm buried oxide). This doped SOI provides the source of silicon for the $\mu$s-Si. To produce this $\mu$s-Si, we spin cast a spin-on glass (SOG) solution (Filmtronic) onto a SOI wafer and exposed it to rapid thermal annealing (RTA) at 700 °C for 4 min to form a uniform film (300 nm thickness). Etching [6:1 buffered oxide enchant (BOE) for 50 s] through a lithographically patterned layer of photoresist (Shipley 1805) opened source and drain windows in the SOG. After stripping the resist, we uniformly deposited a phosphorus containing SOD (Filmtronic) by spin casting. RTA at 950 °C for 5 s caused the phosphorus from the SOD to diffuse through the lithographically defined openings in the SOG and into the underlying silicon. The SOG blocked diffusion in the other areas. The wafer was rapidly cooled to room temperature, immersed in BOE for 90 s to remove both the SOG and SOD and then thoroughly washed with DI water to complete the doping process.

We used techniques described previously to create the $\mu$s-Si and print it onto plastic substrates of PET coated with indium tin oxide (ITO; 100 nm, gate electrode) and epoxy

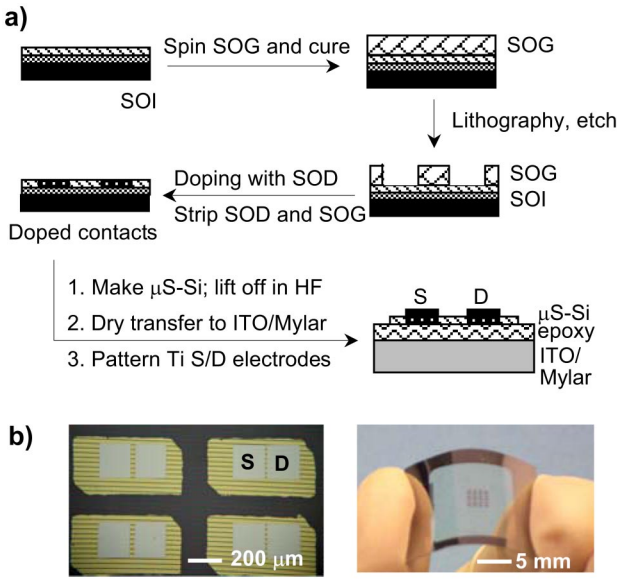


FIG. 1. (Color online) (a) Schematic illustration of process steps for fabricating flexible single crystal silicon transistors with doped contacts on plastic substrates. A spin-on dopant (SOD) provides the phosphorus dopant. A spin-on glass (SOG) serves as a mask to control where dopant diffuses into the silicon. After doping, the silicon is removed from the wafer and transfer printed onto a plastic substrate where device fabrication is completed; (b) optical images of an array of devices on a plastic substrate.

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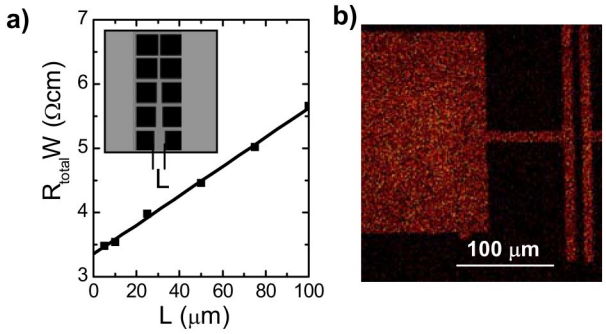


FIG. 2. (Color online) (a) Width normalized resistance ($R_{total}W$) measured between two contacts as a function of L on uniform, highly doped $\mu$s-Si thin film. The intercept of a linear fit to these data gives a contact resistance. Inset shows the test structures for evaluating the contact resistance; (b) phosphorus concentration in a silicon film with patterned doping, as evaluated by TOF-SIMS.

(SU8; 600 nm, gate dielectric).[7] The epoxy not only provides the dielectric, but also facilitates the transfer printing of the $\mu$s-Si.[8] Source and drain electrodes of Ti (100 nm) were formed on the doped contact regions by an aligned photolithography step followed by etch back. Figure 1(b) shows images of several devices.

We estimated the doping levels and the contact resistances using a standard transmission line model (TLM). In particular, we measured resistances between Ti contact pads with separations ($L$) between 5 and 100 $\mu$m and widths ($W$) of 200 $\mu$m [inset in Fig. 2(a)] on uniformly doped $\mu$s-Si on plastic. The linear current ($I$) vs. voltage ($V$) curves (not shown) indicate that the contacts are ohmic and that the doping level is high. The dependence of the resistance on $L$ can be described by $R_{total}=2R_c+(R_s/W)L$, where $R_{total}$ ($=V/I$) is the resistance between two contact pads, $R_c$ is the contact resistance, and $R_s$ is the sheet resistance.[9] Figure 2(a) plots the normalized resistance, $R_{total}W$, as a function of $L$. Linear fitting of $R_{total}W$ gives $R_s=228\pm5\ \Omega/\mathrm{sq}$, and $R_cW \sim 1.7\pm0.05\ \Omega\,\mathrm{cm}$. The value of normalized contact resistance $R_cW$ is more than an order of magnitude lower than what we observed for undoped $\mu$s-Si processed in a similar manner.[7] The resistivity is about $2.3\times10^{-3}\ \Omega$ cm, which corresponds to a doping level of $10^{19}/\mathrm{cm}^3$ if we assume, for simplicity, that the doping is uniform through the 100 nm $\mu$s-Si film. As illustrated by the time-of-flight secondary ion mass spectroscopy (TOF-SIMS) measurements in Fig. 2(b), the use of patterned SOG as a diffusion barrier (Fig. 1) localizes the dopants to desired regions in the silicon. In this image, the bright red color indicates high phosphorus concentration.

Figure 3 shows measurements of typical contact-doped $\mu$s-Si transistors on an epoxy/ITO/PET substrate. Figure 3(a) plots the current–voltage characteristics of a device ($L=7\ \mu\mathrm{m}, W=200\ \mu\mathrm{m}$). The effective device mobility ($\mu_{eff}$) is $\sim240\ \mathrm{cm}^2/\mathrm{V\,s}$ in the linear regime and $\sim230\ \mathrm{cm}^2/\mathrm{V\,s}$ in the saturation regime, as determined by application of standard field-effect transistor models.[10] Figure 2(b) shows transfer characteristics of devices with channel lengths between 2 and 97 $\mu$m and channel widths of 200 $\mu$m. The ON to OFF current ratios in all cases are $\sim10^4$. Figure 3(c) presents the resistance of the devices measured in ON state ($R_{on}$) at small drain voltages, and multiplied by $W$, as a function of $L$ at different gate voltages. Linear fits of $R_{on}W$ vs. $L$ at each gate

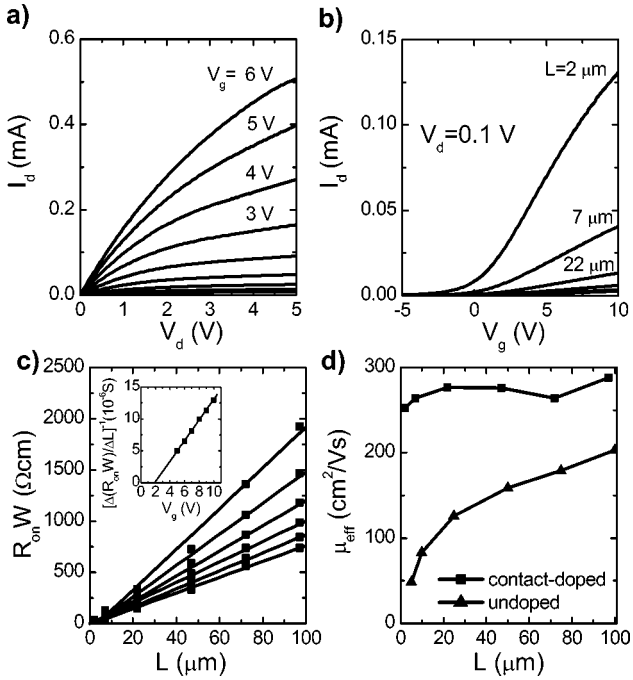


FIG. 3. (a) Typical current–voltage characteristics of a single crystal silicon transistor with doped contacts on a PET substrate, with $L=7\ \mu$m and $W=200\ \mu$m. From bottom to top, $V_G$ varies from −2 to 6 V; (b) transfer curves ($V_d=0.1$ V) of devices with channel lengths, from top to bottom, of 97, 72, 47, 22, 7, and 2 $\mu$m. The channel width in each case is 200 $\mu$m; (c) width-normalized resistance of devices in the ON state ($R_{on}W$) as a function of channel length $L$ at different gate voltages. The solid lines represent linear fits. The scaling is consistent with contacts that have negligible influence on device performance for this range of channel lengths. Inset shows the sheet conductance $[\Delta(R_{on}W)/\Delta L]^{-1}$, determined from the reciprocal of the slopes of the linear fitting in (c), as a function of gate voltage; (d) effective mobility, evaluated in the linear regime, as a function of channel length for the devices with undoped (triangle) and doped (square) contacts.

voltage provide information about both intrinsic device mobility and contact resistance.[9] In this simple model, $R_{on}$ consists of the series addition of the channel resistance (which is proportional to $L$) and the combined contact resistance $R_c$ associated with the source and drain electrodes. Figure 3(c) shows that $R_c$, as determined from the intercepts of linear fitting, is negligible compared to channel resistance for all channel lengths evaluated. The inset shows the variation of sheet conductance, as determined from the reciprocal of the slope of linear fitting in Fig. 3(c), with gate voltage. The linear fit to these data gives an intrinsic device mobility of $\sim270\ \mathrm{cm}^2/\mathrm{V\,s}$, and an intrinsic threshold voltage of $\sim2$ V.

Figure 3(d) compares the effective mobilities, $\mu_{eff}$, of undoped and contact-doped $\mu$s-Si transistors evaluated directly from transfer characteristics measured in the linear regime (i.e., contact effects are not subtracted). For the undoped devices, $\mu_{eff}$ decreases rapidly from 200 to 50 $\mathrm{cm}^2/\mathrm{V\,s}$ with decreasing the channel length $L$ from 100 to 5 $\mu$m. The contacts begin to dominate device behavior at channel lengths below $\sim50\ \mu$m. In the contact doped case, the mobilities are around 270 $\mathrm{cm}^2/\mathrm{V\,s}$, with $<10\%$ variation with channel length over this range, which is in consistent with the intrinsic device mobility determined from inset of Fig. 3(c). These data provide additional evidence that these devices show negligible effects of contact resistance. We note that, in addition to the different mobilities, the devices with doped contacts are more stable, more

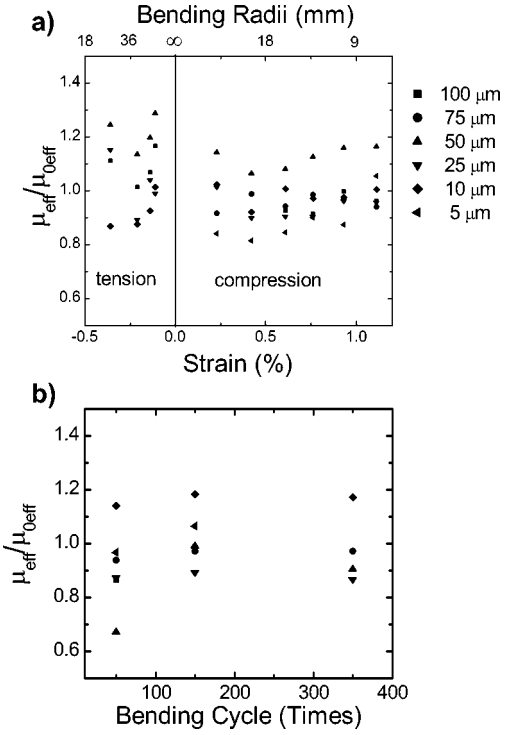


FIG. 4. Bending and fatigue tests of single crystal silicon transistors with doped contacts on flexible PET substrates, for several different channel lengths: (a) normalized effective mobility ($\mu_{\text{eff}}/\mu_{0\text{eff}}$) as a function of bend induced strain (bend radius). Negative and positive strains correspond to tension and compression, respectively; (b) normalized effective mobility after bending (to a radius of 9.2 mm; 0.98% strain) and unbending the devices several hundred times. No significant change in device properties is observed.

uniform in their properties and less sensitive to processing conditions than those with undoped contacts.

Mechanical flexibility is an important characteristic of devices of this type. We performed systematic bending tests on the contact-doped $\mu$s-Si transistors, with bending directions that place the devices in compression and in tension. We also carried out some fatigue tests. The details of the experimental setup can be found elsewhere.[7] Figure 3(a) shows the change of the effective device mobility, normalized by the value in the unbent state, $\mu_{0\text{eff}}$, as a function of strain (or bending radius). Negative and positive strains correspond to tension and compression, respectively. For this range of strains (corresponding to bend radii down to $\sim$1 cm for the 200 $\mu$m thick substrate), we observed only small ($<$20% in most cases) changes in $\mu_{\text{eff}}/\mu_{0\text{eff}}$, the threshold voltage and the on/off ratio. This level of mechanical flexibility is comparable to that reported for organic and *a*-Si transistors on plastic substrates.[11] Figure 4(b) presents the change of $\mu_{\text{eff}}/\mu_{0\text{eff}}$ after several hundred bending cycles that cause compressive strain at the device to vary between 0% and 0.98%. Little change in the properties of the devices was observed; after 350 cycles, the $\mu_{\text{eff}}/\mu_{0\text{eff}}$, the threshold voltage and the on/off ratio change by less than 20%. These results indicate good fatigue stability of $\mu$s-Si transistors.[12]

In summary, this letter demonstrates a spin-on dopant process for contact-doped single crystal silicon transistors on plastic substrates. Scaling analysis indicates that this process yields devices that are not contact limited, which creates the possibility for high frequency silicon devices on plastic substrates. This feature, combined with the remarkably good mechanical flexibility and fatigue stability of the devices, make this contact doped $\mu$s-Si approach a promising potential route to flexible macroelectronic systems.

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[1]G. H. Gelinck, T. C. T. Geuns, and D. M. De Leeuw, Appl. Phys. Lett. **77**, 1487 (2000).
[2]J. A. Rogers, Z. Bao, K. Baldwin, A. Dodabalapur, B. Crone, V. R. Raju, V. Kuck, H. E. Katz, K. Amundson, J. Ewing, and P. Drzaic, Proc. Natl. Acad. Sci. U.S.A. **98**, 4835 (2001).
[3]C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, J. Fancl, and J. West, Appl. Phys. Lett. **80**, 1088 (2002).
[4]For reviews and references, see *Thin Film Transistors*, edited by C. R. Kagan and P. Andry (Dekker, New York, 2003).
[5]E. Menard, K. J. Lee, D.-Y. Khang, R. G. Nuzzo, and J. A. Rogers, Appl. Phys. Lett. **84**, 5398 (2004).
[6]Y. Sun and J. A. Rogers, Nano Lett. **4**, 1953 (2004); Y. Sun, D.-Y. Khang, F. Hua, K. Hurley, R. G. Nuzzo, and J. A. Rogers, Adv. Funct. Mater. **15**, 30 (2005); K. Lee, J. A. Rogers, and R. G. Nuzzo, Appl. Phys. Lett. **86**, 093507 (2005).
[7]E. Menard, R. G. Nuzzo, and J. A. Rogers, Appl. Phys. Lett. **86**, 093507 (2005).
[8]We note that the active interface of the device might lie at the interface between a native $SiO_2$ layer and the Si, rather than between the Si and the epoxy. In this case, the dielectric is a composite, consisting of the native $SiO_2$ and the epoxy. The details represent topics of current study.
[9]S. Luan and G. W. Neudeck, J. Appl. Phys. **72**, 766 (1992).
[10]S. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
[11]T. Sekitani, Y. Kato, S. Iba, H. Shinaoka, and T. Someya, Appl. Phys. Lett. **86**, 073511 (2005); S. H. Won, J. K. Chung, C. B. Lee, H. C. Nam, J. H. Hur, and J. Jang, J. Electrochem. Soc. **151**, G167 (2004).
[12]Note that the devices with doped contact have better fatigue stability than the undoped $\mu$s-Si TFTs.